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10/062,422	02/05/2002	Tsuyoshi Yoneyama	111907	4116

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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	13

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,422	YONEYAMA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004 and 20 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 04/20/2004 and the supplemental amendment filed on 05/20/2004 are entered. The rejections of claims 1-26 are maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-5, 8-12, 14-18, 22-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. As to claims 1-5, 8-12, 14-18, it is not clear what the Applicant means "a plurality of frame selection circuits which are provided in correspondence with the plurality of grayscale pattern selection circuits", lines 8-9 of claim 1.

Specification discloses "the configuration could also be such that each of the grayscale pattern selection ROMs 4A to 4D and the corresponding one of the FRCROMs 5A to 5D are configured as a single ROM," page 25, lines 8-10.

This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how a plurality of frame selection circuits which are provided in correspondence with the plurality of grayscale pattern selection circuits.

4. As to claims 22-26, it is not clear what the Applicant means "a gray scale pattern selection circuit which selects one Frame Rate Control Read Only Memory from among the plurality of Frame Rate Control Read Only Memories," lines 7-8 of claim 22.

Specification discloses "the gray scale pattern selection ROMs 4A to 4D output gray scale pattern selection signals for selecting the one gray scale pattern among the plurality of gray scale patterns stored in the FRCROMs 5A to 5D," page 22, lines 13-16.

This limitation contains various inconsistencies and/or ambiguities so that the Examiner is unable to understand how a gray scale pattern selection circuit which selects one Frame Rate Control Read Only Memory from among the plurality of Frame Rate Control Read Only Memories.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 20, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Kudo et al (US 6,353,435).

As to claim 20, Kudo et al teaches a display driver circuit associated with a method, the display driver circuit comprising

[recited in lines 2-4 of claim 20]

The FRC decoders 101 to 104 include an FRC pattern generator 107 for generating indicate on/off data for generation of 64 types of FRC patterns associated with bits (6 bits) of the gray-scale data per pixel, and a selector 108 for selecting one of the 64

types of indicate on/off data generated by the FRC pattern generator 107 (col. 9, lines 33-38).

The FRC patterns shown in FIG. 6 are arranged to be switched on a frame basis with use of 10 frames as one FRC period. Accordingly, the FRC patterns shown by P-F11 to P-F16 are the same as the FRC patterns shown by P-F1 to P-F6 (col. 10, lines 59-63) meet the claimed limitation "a plurality of grayscale pattern with mutually different frame cycles."

[recited in lines 5-6 of claim 20]

As shown in FIG. 3, further, the FRC decoders 101 to 104 generates indicate on/off data for formation of an FRC pattern to be output at a frame previous by 2 frames each time the Vsync count value issued from the Vsync counter 105 is incremented by 1; and generates indicate on/off data for formation of an FRC pattern to be output at a frame previous by 4 frames each time the Vsync count value is reset, i.e., is switched from "3" to "0" (col. 9, line 64 through col. 10, line 4).

As to claim 21, Kudo et al teach a data width conversion (22) (an image data conversion circuit) which receives 6 bits data, converts the 6 bits data into 16 bits data grayscale pattern and supplies the 16 bits data to the line memory group A (23) (figure 2, column 8, lines 16-25).

The FRC decoders 101 to 104 include an FRC pattern generator 107 for generating indicate on/off data for generation of 64 types of FRC patterns associated with bits (6 bits) of the gray-scale data per pixel, and a selector 108 for selecting one of

the 64 types of indicate on/off data generated by the FRC pattern generator 107 (col. 9, lines 33-38).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 7, 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo et al (US 6,353,435) in view of Bassetti, Jr. (US 5,122,783).

As to claim 6, Kudo et al teaches a display driver circuit comprising

a frame memory 8 (Random Access Memory, figure 1),

[recited in lines 4-7 of claim 6]

That is, the 64 types of gray-scale pattern generators of the FRC pattern generator 107 (see FIG. 4) of the FRC decoder 101 corresponding in number to the gray-scale data bits are set to generate, according to the Vsync count value, indicate on/off data for formation of FRC patterns to be output at the first (Vsync count value=0), third (Vsync count value=1), fifth (Vsync count value=2) and seventh (Vsync count value=3) ones of frames included in the FRC period, with respect to pixels specified by the signals Vsync, Hsync and DotCK applied to the FRC decoder 101 (col. 10, lines 12-20).

[recited in lines 8-10 of claim 6]

The FRC decoders 101 to 104 include an FRC pattern generator 107 for generating indicate on/off data for generation of 64 types of FRC patterns associated with bits (6

bits) of the gray-scale data per pixel, and a selector 108 for selecting one of the 64 types of indicate on/off data generated by the FRC pattern generator 107 (col. 9, lines 33-38).

[recited in lines 11-12 of claim 6]

As shown in FIG. 3, further, the FRC decoders 101 to 104 generates indicate on/off data for formation of an FRC pattern to be output at a frame previous by 2 frames each time the Vsync count value issued from the Vsync counter 105 is incremented by 1; and generates indicate on/off data for formation of an FRC pattern to be output at a frame previous by 4 frames each time the Vsync count value is reset, i.e., is switched from "3" to "0" (col. 9, line 64 through col. 10, line 4).

Kudo et al fails to teach the Random Access Memory is electrically connected to the plurality of gray scale pattern selection circuits.

Bassetti teaches RAM 1080 is directed through at least one of two or more gray scale generated units (fig. 10a, col. 17, lines 14-16). RAM 1080 is also applied to a gray scale unit selecting module 910 which decides which of the two or more gray scaling units 800, 875 or 970 (col. 17, lines 21-24).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Kudo's memory which is directed through at least one of two or more gray scale pattern selection units, in view of the teaching in Bassetti's reference because this would provide the mapping function of the brightness-spreading RAM 1080 are downloaded from the CPU 880 as taught by Bassetti (col. 17, lines 11-13).

As to claim 7, Kudo et al teach a display drive circuit associated with a method comprising a data width conversion (22) (an image data conversion circuit) which receives 6 bits data, converts the 6 bits data into 16 bits data grayscale pattern and supplies the 16 bits data to the line memory group A (23) (figure 2, column 8, lines 16-25); a plurality grayscale No. 1 to No. 64 pattern generator correspond to a plurality of selectors (108) (figure 4, column 10, lines 12-50).

As to claim 13, Kudo et al teach a liquid crystal controller (3) (a drive signal circuit), a liquid crystal display (9) (a terminal outputs a drive signal, figure 1, column 7, lines 25-37).

As to claim 19, Kudo et al teach column drivers (504, 505), and row drivers (502, 503) (figure 48) which mutually intersect pixels.

Response to Arguments

8. Applicant's arguments filed 4/20/2004 and 5/20/2004 have been fully considered but they are not persuasive.

9. In response to applicant's argument (amendment filed on 4/20/2004 and supplemental amendment filed on 5/20/2004) of claims 1-5, 8-12, 14-18, 22-26. This argument is not persuasive because of the rejections stated in paragraphs 3 and 4 above.

In response to applicant's argument (amendment filed on 4/20/2004) that claim 6 recites "a plurality of Frame Rate Control Read Only Memory which store a plurality of grayscale pattern with mutually different frame cycles, and used data stored in RAM to select one grayscale pattern from among the plurality of grayscale pattern."

This argument is not persuasive because Examiner clarifies the teaching of Kudo et al recited in col. 10, line 9 through col. 31 meet the claimed limitation of claim 6, lines 4-7.

For example, FRC decoders A to D (101 to 104) (fig. 3) correspond to the plurality of Frame Rate Control Read Only Memory as claimed.

Fig. 4 shows gray scale No. 1 to No. 64 pattern generator which is detailed of FRC decoders A to D (101 to 104).

The FRC patterns shown in FIG. 6 are arranged to be switched on a frame basis with use of 10 frames as one FRC period. Accordingly, the FRC patterns shown by P-F11 to P-F16 are the same as the FRC patterns shown by P-F1 to P-F6 (col. 10, lines 59-63) meet the claimed limitation "a plurality of grayscale pattern with mutually different frame cycles."

6 denotes a frame rate control (FRC) establish memory for storing therein gray-scale data for gray-scale control, 8 denotes a frame memory for storing therein indicate data included in the digital video signal (col. 7, lines 27-31) meet the claimed limitation "use data stored in the Random Access Memory.

The FRC decoders 101 to 104 include an FRC pattern generator 107 for generating indicate on/off data for generation of 64 types of FRC patterns associated with bits (6 bits) of the gray-scale data per pixel, and a selector 108 for selecting one of the 64 types of indicate on/off data generated by the FRC pattern generator 107 (col. 9, lines 33-38) meet the claimed limitation "select one gray scale pattern from among the plurality of gray scale patterns."

10. In response to applicant's argument (supplemental amendment filed on 5/20/2004) that claim 6 recites "the Random Access Memory is electrically connected to a plurality of grayscale pattern selection circuits." This argument is not persuasive because Bassetti teaches RAM 1080 is directed through at least one of two or more gray scale generated units (fig. 10a, col. 17, lines 14-16). RAM 1080 is also applied to a gray scale unit selecting module 910 which decides which of the two or more gray scaling units 800, 875 or 970 (col. 17, lines 21-24).

11. Applicant's argument state that "FRCROMs are frame rate control read only memory circuits, which are not disclosed or taught in Kudo," page 11, two last lines (amendment filed on 4/20/2004). In response, Examiner disagrees because Kudo teaches FRC decoders (ROMs) A to D (101 to 104) (fig. 3) correspond to the plurality of Frame Rate Control Read Only Memory.

12. In response to applicant's argument (supplemental amendment filed 05/20/2004) that claim 20 recited "selecting one grayscale pattern from a plurality of grayscale patterns having at least two types of frame cycles." This argument is not persuasive because Kudo teaches the FRC decoders 101 to 104 generates indicate on/off data for formation of an FRC pattern to be output at a frame previous by 2 frames each time (col. 9, lines 64-67).

For these reasons, the rejections based on Kudo et al and Bassetti, Jr. have been maintained.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
July 28, 2004

XIAO WU
PRIMARY EXAMINER